Department of EEE, BUET, IEEE EDS/SSCS Bangladesh Jt. Chapter, and IEEE EDS SB of BUET

Notice

A talk, jointly organized by the Dept. of EEE, BUET, IEEE EDS/SSCS Bangladesh Jt. Chapter and IEEE EDS Student Branch of BUET, is arranged as per the following schedule:

Date and Time:	26 May, 2025 (Monday) at 3 PM
Venue:	Room no. 634, Dept of EEE, ECE Building, BUET

Title: Designing Secure Chips for AI with AI and Emerging Technologies
Speaker: Dr. Sazadur Rahman, Assistant Professor, ECE, University of Central Florida

You are cordially invited to attend the Talk.

Dr. A. B. M. Harun-Ur-Rashid
Professor and Head
Dept. of EEE, BUET
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Dr. Ahmed Zubair
Professor, Dept. of EEE, BUET
and
Chair, IEEE EDS/SSCS Bangladesh Jt. Chapter

Abstract: Generative design, powered by artificial intelligence (AI) and machine learning, revolutionizes engineering processes. Things that were once manual and labor intensive are now becoming feasible by AI. On the hardware side, heterogeneous integration is revolutionizing the industry by combining diverse components and technologies. Hence, the semiconductor industry is undergoing a transformative shift driven by the integration of AI, large language models and heterogeneous systems. This seminar will explore how AI reshapes the hardware design landscape, enabling intelligent automation, optimization, and prediction across design. Moreover, we will discuss the reliability and security of silicon photonic heterogeneous integration to optimize computing, performance, and efficiency for diverse applications. Finally, the we will address the critical role of confidential computing, specifically, fully homomorphic encryption (FHE) and AI-based threat modeling, in safeguarding intellectual property and sensitive data.

Brief Biography of the Speaker: Dr. Sazadur Rahman is an Assistant Professor in the Department of Electrical and Computer Engineering at the University of Central Florida. He is also affiliated with the CREOL and CS Dept. at UCF under the "Cyber Security and Privacy Cluster." Before joining UCF, Dr. Rahman was a Security Architect at Intel Corporation, working in security hardening and threat modeling of next-generation Xeon processors. He earned his Ph.D. and M.Sc. from the Department of ECE, University of Florida at FICS lab. Earlier, Dr. Rahman received a B.Sc. degree in EEE from BUET. Before starting his graduate studies, Dr. Rahman was a design engineer in different fabless semiconductor companies for 4 years. He has co-authored over twenty peer-reviewed research papers, four patents, one textbook, and several book chapters. His research works are showcased in premier ACM/IEEE journals and conferences, including the Design Automation Conference (DAC), IEEE Hardware Oriented Security and Trust (HOST), Elsevier Integration, etc. He has been a TPC member for numerous IEEE and ACM conferences including DAC, HOST, etc. His research interests include Supply Chain Security, Silicon-photonic Heterogeneous Integration, AI-Assured Chip Design, and data privacy.