Appendix B

i. Resolution of Academic Council Meeting 474, Date 11.01.2022, Resolution no 220148 (Page 17-18 contains the approval that is copied below. Whole resolution is attached)

প্রস্তাব নং ২২০১৪৮ ঃ গত ০৯-০১-২০২১ ইং তারিখে অনুষ্ঠিত তড়িৎ ও ইলেকট্রনিক কৌশল অনুষদ সভার ২, ৩ ও ৪ নং সিদ্ধান্ত একাডেমিক কাউন্সিলে উপস্থাপনের জন্য তড়িৎ ও ইলেকট্রনিক কৌশল অনুষদের ডীন মহোদয় রেজিস্ট্রার অফিসে প্রেরণ করেন।

সিদ্ধান্ত সমূহ:

(২) সি.এস.ই বিভাগের প্রাক্তন শিক্ষক ড. সৈয়দ মাহবুবুর রহমান বিগত ১৫ই এপ্রিল ২০২১ সালে মিনেসোটায় ইন্তেকাল করেন। সি.এস.ই বিভাগের জি-০৭ হার্ডওয়ার ল্যাবটি তাঁর নামে নামকরন সংক্রান্ত আলোচনা (Meeting number/2021/Term-July/03_Online Date January 1, 2022)।

সিদ্ধান্তঃ আলোচনার পর সিদ্ধান্ত নেয়া হয় যে, প্রফেসর ড. সৈয়দ মাহবুবুর রহমানের সি.এস.ই বিভাগের সূচনালগ্নে বিশেষ অবদানের জন্য সি.এস.ই বিভাগের G-07 ল্যাবরেটরীটি সৈয়দ মাহবুবুর রহমান হার্ডওয়ার ল্যাবরেটরী হিসেবে নামকরন করা হবে। (সংযুক্ত)

(৩) ত. ই কৌশল বিভাগের BUGS এর Meeting No 08.2021 এর সিদ্ধান্ত-২ এর বিষয়ে অনুমোদিত হয় (সংযুক্ত)।

(৪) বায়োমেডিক্যাল ইঞ্জিনিয়ারিং বিভাগের আন্ডারগ্রাজুয়েট কোর্স সিলেবাস পুনর্গঠন সংক্রান্ত (BME বিভাগের BUGS এর ০৮-০৯-২০২১ তারিখের সভার সিদ্ধান্ত) আলোচনা সভায় অনুমোদিত হয় (সংযুক্ত)।

এমতাবস্থায়, অনুষদ সভার ২, ৩ ও ৪ নং সিদ্ধান্ত অনুমোদন বিষয় বিবেচনা।

সিদ্ধান্ত ঃ **(ক) গত ০৯-০১-২০২১ ইং তারিখে অনুষ্ঠিত তড়িৎ ও ইলেকট্রনিক কৌশল অনুষদ সভার ২ ও ৩ নং সিদ্ধান্ত প্রস্তাব মোতাবেক অনুমোদন করা হলো।**

(খ) বায়োমেডিক্যাল ইঞ্জিনিয়ারিং বিভাগের আন্ডারগ্রাজুয়েট কোর্সে ১ (এক) ক্রেডিট Industrial Attachment সংযুক্ত করা এবং অন্যান্য অনুষদের কোন বিভাগের সাথে সম্পর্কিত কোর্স অন্তর্ভূক্ত করলে বা অন্যান্য অনুষদের কোন বিভাগের কোর্স পরিবর্তন করা হয়ে থাকলে সেসব অনুষদের অনুমোদন সাপেক্ষে বায়োমেডিক্যাল ইঞ্জিনিয়ারিং বিভাগের প্রস্তাবিত সিলেবাস অনুমোদন দেয়া হলো। প্রস্তাবিত সিলেবাস ২০২০-২০২১ শিক্ষাবর্ষের লেভেল-১, টার্ম-১ থেকে চালু করা হবে।

পরিশেষে, সভাপতি মহোদয় সভায় উপস্থিত সকলকে ধন্যবাদ জানিয়ে সভার কার্য সমাপ্তি ঘোষণা করেন।

অনুমোদিত।

ii. Proceedings of the BUGS Meeting No. 08/2021 (Date December 17, 2021) (Decision 2 copied below. Entire resolution is attached)

2. The BUGS discussed the proposed elective courses
(i) The BUGS discussed the proposed revised six courses presented by Curriculum Committee and approved as shown in Annexure 1. The BUGS also mentioned that department should take necessary steps to update the relevant laboratories with required equipment following the revised contents. (ii) The BUGS also discussed about committee's capstone project proposal and requested them to prepare the complete proposal and present in next meeting.

iii. Annexure 1 of Proceedings of the BUGS Meeting No. 08/2021

Current Content	Proposed Content
EEE 101 Electrical Circuits I **3 Credit Hours, 3 Contact Hours per Week** Circuit variables: voltage, current, power and energy, Voltage and current independent and depended sources, Circuit elements resistance, inductance and capacitance. Modeling of practical circuits, Ohms law and Kirchhoff's laws, Solution of simple circuits with both dependent and independent sources, Series-parallel resistance circuits and their equivalents, Voltage and current divider circuits, Delta-Wye equivalent circuits, Techniques of general DC circuit analysis (containing both independent and dependent sources): Node-voltage method, Mesh-current method, Source transformations. Thevenin and Norton equivalents, Maximum power transfer. Superposition technique. Properties of Inductances and capacitances. Series-parallel combinations of inductances and capacitances; Concepts of transient and steady state response with dc source. Definitions of ac voltage, current, power, volt-ampere and various factors (including power, peak, form factors etc.) , Introduction to sinusoidal steady state analysis: Sinusoidal sources, phasor, impedance, admittance, reactance, susceptance; voltage, current, power of R, L, C. R-L, R-C, R-L-C circuits with sinusoidal source, Series - parallel and Delta-Wye simplifications of circuits with R, L, Cs. Techniques of general ac circuit analysis (containing both independent and dependent sources): Node-voltage method, Mesh current method, Source transformations, Thevenin and Norton Equivalents, Phasor diagrams. Sinusoidal steady state power calculations, RMS values, Real and reactive power. Maximum power transfer, impedance matching. Steady state voltage, current.	**EEE 101 Electrical Circuits I** **3 Credit Hours, 3 Contact Hours per Week** Basic Concepts, Charge, Current and Voltage, Power and Energy, Circuit Elements, Applications; Basic Laws, Ohm's Law, Nodes, Branches, and Loops, Kirchhoff's Laws, Series Resistors and Voltage Division, Parallel Resistors and Current Division, Solution of simple circuits with both dependent and independent sources, Wye-Delta Transformations, Applications; Nodal and Mesh Analysis, Applications; Linearity Property, Superposition, Source Transformation, Thevenin's and Norton's Theorem, Maximum Power Transfer Theorem. Properties of Inductances and capacitances. Series-parallel combinations of inductances and capacitances; Concepts of transient and First-Order Circuits, The Source-Free RL and RC Circuit, Step Response of an RL and RC Circuit, Second-Order Circuits, Finding Initial and Final Values, The Source-Free Series and Parallel RLC Circuit, Step Response of a Series and Parallel RLC Circuit, Duality, Applications of DC transients. Basic Magnetic Circuits: Magnetic quantities and variables: Field, Flux, Flux Density, Magnetomotive Force, Magnetic Field Strength, permeability and B-H Curve, reluctance, magnetic field strength. Laws in magnetic circuits: Ohms law and Amperes circuital law. Magnetic circuits: Composite series magnetic circuit, parallel and series-parallel circuits. Comparison between electrical and magnetic quantities, Hysteresis and hysteresis loss. Magnetic materials.

EEE 105 Electrical Circuits II **3 Credit Hours, 3 Contact Hours per Week** Circuits with non-sinusoidal excitations, power and power factor of ac circuits with multiple sources of different frequencies; Transients in AC circuits, Passive Filter Networks: basic types. Characteristic impedance and attenuation, ladder network, low pass, high pass filters, propagation coefficient and time delay in filter sections, practical composite filters. Resonance in AC circuits: Series and parallel resonance and Q factors. Magnetically coupled circuits. Analysis of three phase circuits: Three phase supply, balanced and unbalanced circuits, power calculation and measurements, Power factor improvement. Basic Magnetic Circuits: Magnetic quantities and variables: Field, Flux, Flux Density, Magnetomotive Force, Magnetic Field Strength, permeability and B-H Curve, reluctance, magnetic field strength. Laws in magnetic circuits: Ohm‟s law and Ampere‟s circuital law. Magnetic circuits: Composite series magnetic circuit, parallel and series-parallel circuits. Comparison between electrical and magnetic quantities, Hysteresis and hysteresis loss. Magnetic materials.	**EEE 105 Electrical Circuits II** **3 Credit Hours, 3 Contact Hours per Week** Sinusoids and Phasors, Phasor Relationships for Circuit Elements, Impedance and Admittance, Impedance and Admittance, Kirchhoff's Laws in the Frequency Domain, Impedance Combinations, Applications; Sinusoidal Steady-State Analysis, Nodal and Mesh Analysis, Superposition Theorem, Source Transformation, Thevenin and Norton Equivalent Circuits; AC Power Analysis, Instantaneous and Average Power, Maximum Average Power Transfer, Effective or RMS Value, Apparent Power and Power Factor, Complex Power, Conservation of AC Power, Power Factor Correction, Applications; Transients in AC circuits. Three-Phase Circuits, Balanced Three-Phase Voltages, Balanced Wye-Wye Connection, Balanced Wye-Delta, Delta-Delta and Delta-Wye Connection, Power in a Balanced System, Unbalanced Three-Phase Systems, Power Factor Correction, Applications; Magnetically Coupled Circuits, Mutual Inductance, Energy in a Coupled Circuit and Ideal Transformers. Frequency Response, Transfer Function, The Decibel Scale, Bode Plots, Series and Parallel Resonance, Passive Filters; Scaling; Nonsinusoidal periodic Waveforms, Composite Waveforms, Average Power and RMS Values of a Nonsinusoidal periodic Waveform, Circuit Response to a Nonsinusoidal Waveform, Power factor of a non-linear load.

EEE 303 Digital Electronics **3 Credit Hours, 3 Contact Hours per Week** Introduction to number systems and codes. Analysis and synthesis of digital logic circuits: Basic logic functions, Boolean algebra, combinational logic design, minimization of combinational logic. MOSFET Digital circuits: NMOS inverter, CMOS inverter, CMOS logic circuits, Clocked CMOS logic circuits, transmission gates, sequential logic circuits, Memories: classification and architecture, RAM memory cells, Read only memory, data converters, BJT digital circuits: ECL, TTL, STTL, BiCMOS, Design application A static ECL gate. Modular combinational circuit design: pass transistor, pass gates, multiplexer, demultiplexer and their implementation in CMOS, decoder, encoder, comparators, binary arithmetic elements and ALU design. Sequential circuits: different types of latches, flip-flops and their design using ASM approach, timing analysis and power optimization of sequential circuits. Modular sequential logic circuit design: shift registers, counters and their applications. State Machine Design. Asynchronous and synchronous sequential circuits.	**EEE 303 Digital Electronics** **3 Credit Hours, 3 Contact Hours per Week** Introduction to number systems and codes. Analysis and synthesis of digital logic circuits: Basic logic functions, Boolean algebra, combinational logic design, minimization of combinational logic. Introduction to Verilog Hardware Description Language programming and structural and behavioral design of digital systems using VerilogHDL, Verilog Timing analysis and test bench, MOSFET Digital circuits: NMOS inverter, CMOS inverter, CMOS logic circuits, Clocked CMOS logic circuits, transmission gates, sequential logic circuits, BJT digital circuits: ECL, TTL, STTL, BiCMOS, Memories: classification and architecture, RAM memory cells, Read only memory, data converters, Modular combinational circuit design: pass transistor, pass gates, multiplexer, demultiplexer and their implementation in CMOS, decoder, encoder, comparators, binary arithmetic elements and ALU design. Sequential circuits: latches, flip-flops timing analysis and power optimization of sequential circuits. Modular sequential logic circuit design: shift registers, counters and their applications. Asynchronous and synchronous sequential circuits. Dual Inline Packaged and Surface Mount Device (SMD) Integrated Circuits, Introduction to System Integration and Printed Circuit Board design, Design of a Simple-As-Possible (SAP) computer: SAP-1, selected concepts from SAP-2 (jump, call, return).

EEE 415 Microprocessors and Embedded Systems **3 Credit Hours, 3 Contact Hours per Week** Basic components of a computer system. Simple-As-Possible (SAP) computer: SAP-1, selected concepts from SAP-2 and SAP-3 (jump, call, return, stack, push and pop). Evolution of microprocessors. Introduction to Intel 8086 microprocessor: features, architecture, Minimum mode operation of 8086 microprocessor: system timing diagrams of read and write cycles, memory banks, design of decoders for RAM, ROM and PORT. Introduction to Intel 8086 Assembly Language Programming: basic instructions, logic, shift and rotate instructions, addressing modes, stack management and procedures, advanced arithmetic instructions for multiplication and division, instructions for BCD and double precision numbers, introduction to 8086 programming with C language. Hardware Interfacing with Intel 8086 microprocessor: programmable peripheral interface, programmable interrupt controller, programmable timer, serial communication interface, keyboard and display interface (LED, 7 segment, dot matrix and LCD).	**EEE 415 Microprocessors and Embedded Systems** **3 Credit Hours, 3 Contact Hours per Week** Fundamentals of microprocessor and computer design, processor data path, architecture, microarchitecture, complexity, metrics, and benchmark; Instruction Set Architecture, introduction to CISC and RISC, Instruction-Level Parallelism, pipelining, pipelining hazards and data dependency, branch prediction, exceptions and limits, super-pipelined vs superscalar processing; Memory hierarchy and management, Direct Memory Access, Translation Lookaside Buffer; cache, cache policies, multi-level cache, cache performance; Multicore computing, message passing, shared memory, cache-coherence protocol, memory consistency, paging, Vector Processor, Graphics Processing Unit, IP Blocks, Single Instruction Multiple Data and SoC with microprocessors. Simple Arm/RISC-V based processor design with VerilogHDL Introduction to embedded systems design, software concurrency and Realtime Operating Systems, Arm Cortex M / RISC-V microcontroller architecture, registers and I/O, memory map and instruction sets, endianness and image, Assembly language programming of Arm Cortex M / RISC-V based embedded microprocessors (jump, call-return, stack, push and pop, shift, rotate, logic instructions, port operations, serial communication and interfacing), system clock, exceptions and interrupt handling, timing analysis of interrupts, general purpose digital interfacing, analog interfacing, timers: PWM, real-time clock, serial communication, SPI, I2C, UART protocols, Embedded Systems for Internet of Things (IoT)
	EEE 466 Analog Integrated Circuits Laboratory **1.5 Credit Hours, 3 Contact Hours per Week** This course consists of two parts. In the first part, students will perform experiments to verify practically the theories and concepts learned in EEE 465. In the second part, students will design simple systems using the principles learned in EEE 465.

EEE 453 VLSI Circuits and Design I **3 Credit Hours, 3 Contact Hours per Week** IC trends, technology and design approaches. MOS device: structure, operation, threshold voltage and characteristics. Ratioed circuits: NMOS inverter with resistive and transistor load, Pseudo NMOS inverter. Ratioless circuits: CMOS inverters: operation, transfer characteristics, design for equal rise and fall time, propagation delay, rise time, fall time and power consumption estimation. NMOS pass transistor and CMOS pass gate circuits. Buffer chain design to drive large capacitive load. Integrated circuit fabrication technology: photolithography, CMOS process flow, design rules. Estimation of resistance and capacitance from layout. Layout matching. Stick diagram and area estimation from stick diagram. Reliability issues: Latch-up, electromigartion. Basic logic gates in CMOS. Synthesis of arbitrary combinational logic in CMOS, pseudo-NMOS, dynamic CMOS, clocked CMOS and CMOS domino logic. Structured design: Parity generator, bus arbitration logic, multiplexers-based design, programmable logic array (PLA) design. Clocked sequential circuit design: two phase clocking, dynamic shift register. CMOS latches and flip flops. Subsystem design: 4-bit arithmetic processor: bus architectures, shifter, design of a general purpose ALU. Memory elements design: System timing consideration, three transistor and one transistor dynamic memory cell. Pseudo-static RAM/register cell. 4 transistors dynamic and 6 transistor static CMOS memory cell. 4x4 bit register array and 16 bit static CMOS memory array. Finite State Machine design: Design of Moore Type and Mealy type FSM using Verilog. Testing VLSI circuit	**Drop the course.**
EEE 454 VLSI Circuits and Design I Laboratory	**Drop the Course**

EEE 457 VLSI Circuits and Design II **3 Credit Hours, 3 Contact Hours per Week** Scaling of MOS transistor and interconnect: RC delay modeling, repeaters and cascaded drives. Advanced CMOS nanometer process flow and enhancement of CMOS process, technology related CAD issues and manufacturing issues, design margin and PVT corners. Circuit characterization: delay estimation and transistor sizing for minimum delay, crosstalk and noise analysis. High speed digital circuit design techniques, circuit families. Architecture for high-speed design: Carry select, carry skip, carry look ahead and tree adders. Modified Booth algorithm, Wallace tree multiplication. Sequential circuit design: sequencing methods, maximum and minimum delay constrains, clock skew. Design of latches and flip-flops, clock Generation and synchronization, High-speed clock generation and distribution. ASIC Cell based design, standard cell place and route design, timing directed placement design, mixed signal design. Interchange formats: LEF, DEF, SDF, DSPF, SPEF, ALF PDEF,CIF and GDS2. Floor planning, power distribution and I/O design. Algorithm and architecture for digital processors in verilog, system verilog and system-C : building block for signal processors, digital filters and signal processors, pipelined architecture. Architecture for arithmetic processors: addition, subtraction, multiplication and division. Complete design of a simple RISC processor. Post-synthesis design validation: timing verification, fault simulation and testing, design for test. High speed and low power memory circuit design: advanced topics in DRAM and SRAM.	**EEE 467 VLSI Circuits and Design** **3 Credit Hours, 3 Contact Hours per Week** Review of Basic CMOS circuits. Scaling of MOS transistor and interconnect: RC delay modeling, repeaters and cascaded drives. Buffer chain design to drive large capacitive load. Logical efforts of paths and the best number of stages. Integrated circuit fabrication technology: photolithography, CMOS process flow, design rules. Advanced CMOS nanometer process flow and enhancement of CMOS process, technology related CAD issues and manufacturing issues, design margin and PVT corners. Reliability issues: Latch-up, electro-migration. Structured design of VLSI circuits: Clocked sequential circuit design: two phase clocking, dynamic shift register. High speed digital circuit design techniques: circuit families, architecture for high speed design, Carry select, carry skip, carry look ahead and tree adders. Wallace tree multiplication. Sequential circuit design: sequencing methods, maximum and minimum delay constrains, clock skew. Design of latches and flip-flops, clock Generation and synchronization, High-speed clock generation and distribution. Memory elements design: SRAM and DRAM design. System timing consideration, static and dynamic CMOS memory array. Finite State Machine design: Design of Moore Type and Mealy type FSM. Digital system design using Verilog, design of a simple RISC processor. Functional verification of digital system using system Verilog: Flat and layered test benches, verification coverage, random test pattern generation and UVM. ASIC Cell based design, standard cell place and route design, timing directed placement design. Floor planning, power distribution and I/O cell placement.
EEE 458 VLSI Circuits and Design II Laboratory **1.5 Credit Hours, 3 Contact Hours per Week** This course consists of two parts. In the first part, students will perform experiments to verify practically the theories and concepts learned in EEE 457. In the second part, students will design simple systems using the principles learned in EEE 457.	**EEE 468 VLSI Circuits and Design Laboratory** **1.5 Credit Hours, 3 Contact Hours per Week** This course consists of two parts. In the first part, students will perform experiments to verify practically the theories and concepts learned in EEE 467. In the second part, students will design simple systems using the principles learned in EEE 467.

Course Equivalent Table:

Old Course	Equivalent New Course
EEE 453 VLSI Circuits and Design I	**EEE 467 VLSI Circuits and Design**
EEE 454 VLSI Circuits and Design I Laboratory	**EEE 468 VLSI Circuits and Design Laboratory**
EEE 457 VLSI Circuits and Design II	**EEE 467 VLSI Circuits and Design**
EEE 458 VLSI Circuits and Design II Laboratory	**EEE 468 VLSI Circuits and Design Laboratory**

Note : If a student want to retake both EEE 453 and EEE 457 or both EEE 454 and EEE458 of the old syllabus, he has to take EEE 467 or EEE 468 of the new syllabus and he must take another optional course from Electronics or interdisciplinary group which he has not previously taken.