Course Content for New Post Graduate Courses of Department of EEE, BUET

Faculty of EEE Meeting No 2025/01, Date: 25.01.2025

EEE 6402: Hardware Security
Division: EP, 3.0 Credit Hour

Introduction, Traditional and Globalized IC Design Flow; The Emergence of Hardware Security Threats: IP Piracy, Overbuilding, Hardware Trojans, Counterfeiting, Reverse Engineering; Design-for-Trust Solutions: Watermarking and Fingerprinting, Camouflaging, Split Manufacturing, Metering, Logic Locking or Obfuscation, IC Design Flow with Logic Locking; Classification of Logic Locking and Attacks, Pre-SAT Logic Locking: Random Logic Locking (RLL), Fault-Analysis Based Logic Locking (FLL), Sensitization Attack, Strong Logic Locking (SLL); Boolean Satisfiability Attack (SAT): Circuit for implementing SAT Attack, Efficient Method of Implementing SAT Attack, Illustration of SAT Attack, Algorithm of SAT Attack; Post-SAT- Point Function-Based Logic Locking: SAT Attack Resistant Logic Locking (SARLock), Construction of SARLock, Security Analysis, Anti-SAT Based Logic Locking, Configurations of Anti-SAT, Finding Lower Bound of SAT Attack on Anti-SAT, Integrating a Circuit with Anti-SAT, Combined with Conventional Logic Locking Techniques, Anti-SAT Block Obfuscation - Removal Attacks, AND-Tree Detection, Logic Locking Attacks; Approximate Attacks: App-SAT, Double-DIP; Structural Attacks: Signal Probability Skew (SPS) attack, AppSAT-Guided Removal (AGR) Attack, Sensitization-Guided SAT (SGS) Attack, Bypass Attack, Cyclic Logic Locking; Algorithmic Attacks: CycSAT, Stripped-Functionality Logic Locking (SFLL), SFLL-HD, SFLL-Flex; Side-Channel Attacks: Differential Power Analysis (DPA) Attack, Test-Data Mining (TDM) Attack, Hill Climbing Search Attack, De-synthesis Attack; Attack-Defense Matrix.

EEE 6516: Quantum Computing
Division: EP, 3.0 Credit Hour

Introduction to quantum computing; Postulates of quantum mechanics; Qubits and single-qubit gates; Operators and quantum measurement; Quantum information processing, superposition, entanglement, no cloning theorem, and quantum teleportation; Quantum circuits, controlled operation and measurement, universal quantum gates; Quantum algorithms: Deutsch-Jozsa algorithm, Grover's algorithm, Shor's algorithm, quantum Fourier transform and phase estimation; Density matrices and Bloch sphere representation of quantum variables; Quantum error correction and fault-tolerant architecture; Physical realization of quantum computers: harmonic oscillator, optical quantum computers, trapped ions, superconducting qubits, and new implementation schemes.

EEE 6617: Privacy Preserving Machine Learning
Division: CSP and Interdisciplinary, 3.0 Credit Hour

Review of common machine learning algorithms; mathematical definition of privacy; case studies of high-profile privacy breaches; common attack and threat models; differential privacy (DP); other privacy approaches; basic building blocks of privacy-preserving algorithm design; achieving DP via noise for numeric queries; achieving DP via sampling for non-numeric queries; the Gaussian mechanism; composition of multi-stage differentially private algorithms; differentially private empirical risk minimization; differentially private stochastic gradient descent; differential privacy for distributed data and federated learning; differential privacy for neural networks; local differential privacy; differentially private heavy hitters; emerging applications; machine unlearning.

EEE 6518: Power Management Integrated Circuits
Division: EP and EEPS, 3.0 Credit Hour

Introduction to Power Management Integrated Circuit (PMIC); Bipolar-CMOS-DMOS (BCD) technology, Scaling trend of BCD technologies, BCD Bulk vs BCD-SOI; Kelvin Sensing; Droop Compensation; Error Amplifier Design; Brokaw Bandgap Circuit, Sub-1V Bandgap Reference; Linear regulator design, PMOS LDO, NMOS LDO, PSSR of PMOS and NMOS LDO; Multiphase Converter; Compensator design using Gm-C architecture; On-Chip-Inductor Design; Hysteretic converter; OLED display driver; Li-ion battery and its charging phases; Design of a battery charger IC; PMIC layout techniques; GaN and SiC power devices; GaN based PMIC design.